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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,186	04/22/2004	Simon C. Steely JR.	200310150-1	6058

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,186	STEELY, SIMON C.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement received April 22, 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Information Disclosure Statement is being considered by the examiner.

Claim Objections

2. Claims 5 and 11 objected to because of the following informalities:

In claim 5, line 3, it appears the language "each segments" should be changed to "each segment". Appropriate correction is required.

In claim 11, line 3, it appears the language "storing, replacement data" should be changed to "storing replacement data". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5 and 7-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Bennett (US PGPub No. 20030204664).

For claim 1, Bennett discloses a method for storing replacement data in a multi-way associative cache (a cache with N elements all simultaneously searched is called an N-way set associative cache, and the N-elements which are chosen for the comparison are called a set of elements, par. 0006; the invention relates to optimizing the operation of a cache through multiway steering for cache access and modified cyclic reuse for cache allocation, par. 0001), comprising:

logically dividing the cache's cache sets into segments of at least one cache way (par. 0001);

searching a cache set in accordance with a segment search sequence for a segment currently comprising a way which has not yet been accessed during a current cycle of the segment search sequence (each cache element or cache cell has a usage bit, if the bit if set, then the cell is in use, and an in-use cell has been accessed at least once since the last time the replacement module cycled through the cache, after an in-use cache cell is access by the replacement module, the usage bit is reset or cleared, and the replacement module advances to the next cache cell, this continues until a cache cell is found where the usage bit is already clear, par. 0028; the search is "content addressable" or "fully associative", which means that all cache elements are searched, and the search my be parallel, by broadcasting current parameters to every element and including a copy of the machinery to match against prior parameters in

every element, or the search may be serial, checking each element against the current parameters using a single copy of the comparison machinery, par. 0005);

searching the current segment in accordance with a way search sequence for a way which has not yet been accessed during a current way search cycle (par. 0028); and

storing the replacement data in a first way which has not yet been accessed during a current cycle of the way search sequence (the replacement module then stores in the first available cache cell the new answer retrieved by the underlying search, par. 0028).

Claim 2 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 3 is rejected using the same rationale as for the rejection of claim 1 above.

For claim 4, Bennett discloses the invention as per rejection of claim 1 above.

Bennett further discloses selecting for replacement consideration a next sequential segment in the segment search sequence (the cyclic replacement module is made up of the advance and select operation, the usage bit test operation, the replace element operation and the clear operation and begins its operation advancing the cyclic counter one count to select the next cache element from the cache array, par. 0043).

Claim 5 is rejected using the same rationale as for the rejection of claim 4 above.

Claim 7 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 8 is rejected using the same rationale as for the rejection of claim 1 above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bennett (US PGPub No. 20030204664) and Johnson (US Patent No. 6,275,919).

For claim 6, Bennett discloses the invention as per rejection of claim 1 above.

Bennett fails to disclose the limitations of the current claim.

Johnson, however, helps disclose repeating the segment search sequence when all segments of the cache set are determined to comprise ways which have been accessed during the current segment search cycle (if the data at an index of a cache memory generated by a current hashing function does not match incoming data, previous hashing functions are used to repeat the search, abstract).

Bennett and Johnson are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include repeating a search for data in a cache because this would provide an improved memory management strategy for us in memories that store and retrieve information based on hash values (col. 2, lines 3-5), as taught by Johnson.

7. Claims 9-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bennett (US PGPub No. 20030204664) and Liu (US PGPub No. 20020138648).

For claim 9, Bennett discloses the invention as per rejection of claim 1 above.

Bennett fails to disclose the limitations of the current claim.

Liu helps disclose prior to the searching of the cache set, determining whether a way of the cache set contains invalidated data and storing the replacement data in the way containing the invalidated data (each valid bit in the validity table can be mapped to an associated directory entry of a set in the address lookup table, a valid bit of binary '0' represents that the associated way of entry in the address lookup table is invalid, par. 0022).

Bennett and Liu are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include determining of invalidated data ways because this would help to indicate the memory space of an associated entry in an address lookup table is idle and can be provided for use (par. 0022), as taught by Liu.

For claim 10, the combined teachings of Bennett and Liu disclose the invention as per rejection of claim 9 above.

Liu further helps disclose storing replacement data in an invalidated way, if any, in the cache set, in response to a cache miss, and setting, in response to a processor accessing the replacement data, a way access indicator corresponding to the accessed way to a value indicating the way has been accessed (a tag stored in the cache directory entry for a set is used to determine whether there is a cache hit or miss for that

set to verify whether the cache line in the set to which a particular memory address is mapped contains the information corresponding to that memory address, par. 0006).

For claim 11, the combined teachings of Bennett and Johnson disclose the invention as per rejections of claims 1 and 10 above.

Bennett further discloses a processing environment comprising a processor, a multi-way associative cache, and a cache controller (the cache system may be in a computer system with at least one processor and a memory, par. 0030; a separate processor could be used as a storage system controller, and the operations of the cache system could be performed, par. 0030).

Claim 12 is rejected using the same rationale as for the rejections of claims 1 and 10 above.

Claim 13 is rejected using the same rationale as for the rejections of claims 7 and 10 above.

Claim 14 is rejected using the same rationale as for the rejections of claims 7 and 10 above.

Claim 15 is rejected using the same rationale as for the rejections of claims 5 and 10 above.

Claim 16 is rejected using the same rationale as for the rejections of claims 10 and 12 above.

Claim 17 is rejected using the same rationale as for the rejections of claims 10 and 11 above.

Claim 18 is rejected using the same rationale as for the rejections of claims 11, 15 and 17 above.

Claim 19 is rejected using the same rationale as for the rejections of claims 11, 15 and 17 above.

Claim 20 is rejected using the same rationale as for the rejections of claims 7, 15 and 17 above.

Claim 21 is rejected using the same rationale as for the rejections of claims 7, 15 and 17 above.

Claim 22 is rejected using the same rationale as for the rejection of claim 17 above.

Claim 23 is rejected using the same rationale as for the rejections of claims 18 and 22 above.

Claim 24 is rejected using the same rationale as for the rejections of claims 19 and 22 above.

Claim 25 is rejected using the same rationale as for the rejections of claims 20 and 22 above.

Claim 26 is rejected using the same rationale as for the rejections of claims 21 and 22 above.

Citation of Pertinent Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Coyle et al (US Patent No. 5,367,653) discloses a reconfigurable set associative cache memory including partitioning for the highest number of ways in a multi-way associative cache.

Rowlands et al (US PGPub No. 20040153607) discloses a cache is configured to receive direct access transactions, which may be used to perform testing of the cache memory.

York (US Patent No. 6,745,291) discloses an n-way set associate data cache system comprises a cache controller adapted to receive a request for data and instructions, and page tags used for comparison with page entry addresses in directories.

Robinson (US PGPub No. 20040078524) discloses a method and structure for replacing cache lines in a computer system having a set associative cache memory.

Contact Information

9. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

4-28-06

PIERRE VITAL
PRIMARY EXAMINER